

REMARKS

Applicant respectfully requests reconsideration of this application. Claims 1-29 are pending. Claims 7, 9, 11-13, 15, and 17-29 have been amended. Claim 1-6, 10, and 16 have been cancelled without prejudice. No claims have been added. Therefore, claims 7-9, 11-15, and 17-29 are now presented for examination.

35 U.S.C. § 102

Olarig, et al.

The Examiner rejected claims 1-29 under 35 U.S.C. § 102 (e) as being anticipated by U.S. Patent Publication No. 2003/0065886 of Olarig et al. (Olarig).

The claims have been modified in response to the rejection. As amended herein, claim 7 reads as follows:

7. A processor comprising:
 - a processor core; and
 - a cache memory for general-purpose operation of the processor core;

wherein the processor is to evaluate the cache memory when a first computer process associated with a thread results in a cache operation for the cache memory to determine whether a dedicated cache for the thread exists in the cache memory and, if a dedicated cache does not exist, whether a dedicated cache for the thread is needed; and

wherein if the processor determines that a dedicated cache for the thread does not exist and a dedicated cache is needed for the thread, the processor is to create a dedicated sector in the cache memory, the resulting cache memory having a first sector for the general purpose operation and a second sector dedicated to the thread.

The Applicant respectfully submits that Olarig does not contain the elements of the claims, as amended herein. In particular, it is submitted that Olarig does not provide for a determination whether a dedicated cache memory exists, or a determination whether a dedicated cache for a thread, is needed when a computer operation associated with a thread is encountered.

Olarig addresses thread operations in certain comments, but does not address the determinations regarding the creation of a dedicated cache in response to a program thread. For example, Olarig indicates the following regarding program threads:

Modern operating systems can issue multiple threads and processes that may share a cache. When a thread or process is preempted, the new thread or process could replace the cache contents of the previous thread or process. When the original thread or process returns, its memory ranges may no longer be cached. The original thread or process may then cache its memory ranges and replace what was cached by the previous thread or process.

(Olarig, ¶ 0008)

Multi-processor computer systems in which multiple processors share a cache also greatly contribute to cache thrashing. For instance, a context switch may occur that shifts to a process for a processor after a previous process for a different processor was cached. Similarly, when logical processors become available from a single physical processor package, threads or processes for one logical processor will likely preempt previous threads or processes of another logical processor and replace the cache contents of these previous threads or processes.

(Olarig, ¶ 0009)

Other examples of entities that can be allocated dedicated cache partitions include processes, threads and nodes. ...

(Olarig, ¶ 0019)

A partitioned cache represents a departure from traditional cache organization. Each cache partition acts as a private cache for its assigned entity. In other words, an entity has certain exclusive rights in its assigned cache partition. This avoids any entity having its cached data thrashed by another entity. This may be particularly advantageous for entities with substantially unrelated processes or threads.

(Olarig, ¶ 0020)

Thus, Olarig recognizes the operation of threads in computer operations in this regard, but Olarig does contain any teaching regarding actions that may be taken with regard to the existence or nonexistence of a dedicated cache when a computer operation associated with a thread is encountered. Specifically, Olarig does not provide for a processor to evaluate a cache memory when a computer process associated with a thread results in a cache operation for the cache memory to determine whether a dedicated cache for the thread exists in the cache memory and, if a dedicated cache does not exist, whether a dedicated cache for the thread is needed. Further, Olarig does not provide for creation of a dedicated cache for a thread if there is a determination that a dedicated cache is needed for the thread.

Olarig does not contain every element of claim 7 and thus claim 7 is not anticipated by Olarig. Independent claims 13, 20, and 25 are allowable for similar reasons. The remaining claims, while having other differences, are dependent claims that allowable as being dependent on the allowable base claims.

With regard to certain specific dependent claims, it is submitted that Olarig does not contain the elements of claim 9, which has been modified for clarity to provide that the first computer process is allocated a subset of the computing cycles of the processor. The Examiner has cited to Figure 4 of Olarig for the rejection of this claim, but it is submitted that this figure is not relevant to this claim. The description of the figure refers to reallocation cycles or iterations, but these are cycles in the process of reallocating the partitioned caches. This is not relevant to a thread that has been allocated a subset of computing cycles of a processor. It is further submitted that claim 15 is allowable for similar reasons.

Conclusion

Applicant respectfully submits that the rejections have been overcome by the amendment and remark, and that the claims as amended are now in condition for allowance. Accordingly, Applicant respectfully requests the rejections be withdrawn and the claims as amended be allowed.

Invitation for a Telephone Interview

The Examiner is requested to call the undersigned at (503) 439-8778 if there remains any issue with allowance of the case.

Request for an Extension of Time

The Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17 for such an extension.

Charge our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 4/25/05



Mark C. Van Ness
Reg. No. 39,865

12400 Wilshire Boulevard
7th Floor
Los Angeles, California 90025-1026
(503) 439-8778